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EXAMINER	
MCCOMMAS, STUART S	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,381	CHILDS ET AL.	
	Examiner	Art Unit	
	Stuart McCommas	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-8, 11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-6, 8 and 10-22 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Inukai (United States Patent 6,680,577), hereinafter referenced as Inukai, in view of Hirane et al. (United States Patent 4,967,192), hereinafter referenced as Hirane.

Regarding claim 1, Inukai discloses an EL display device 101 including an array of display pixels 104 (figure 1A) where each pixel includes an EL display element 109 and a current source circuit including a transistor 108 and a capacitor 112 (figure 1B) for driving current through the EL display element 109 where the current through the EL display element 109 depends on a data voltage (column 7 lines 45-58), and where the device is operable in several periods within a frame (figures 5A-5F, column 9 lines 29-36). Inukai further discloses that the first period has a first length and that during the first period a first current of a group of currents can be driven through the EL display element 109 (column 9 lines 21-36; figures 5A-5F). Inukai further discloses that the second period has a length different from the first period (Figure 5A-5F) and that during the second period a second current of a plurality of currents is driven through the EL

display element 109 (column 9 lines 21-36) and that the first and second currents of the respective pluralities of drive currents can be selected independently of one another (column 3 lines 61-67; figure 5D). Further Inukai discloses that the current levels, including a zero drive level, and that the duration of one period is approximately n times the duration of the other phase where n is the number of drive currents that can be used in the display(figures 5A-5F; column 3 lines 25-40; column 8 lines 51-55). Further Inukai discloses wherein during said first phase each of the pixel display elements is sequential driven for said first duration with a corresponding one of said first plurality of drive current and during said second phase each of the pixel display elements Is sequential driven for said second duration with a corresponding one of said second plurality of drive currents associated with said second phase (column 3 lines 11-67; column 4 lines 1-19; figures 5A-5E).

However Inukai fails to disclose more than two drive current levels and wherein the first plurality of drive current comprises a number n of drive current levels.

In a similar field of invention Hirane discloses more than two drive current levels or current volumes for a current driving method (column 4 lines 54-67; column 7 lines 48-63; column 8 lines 37-47; figure 3). Further Hirane discloses that the first plurality of drive currents comprises a number n of drive current levels (column 4 lines 54-67; column 7 lines 48-63; column 8 lines 37-47; figure 3; table 1).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inukai with Hirane by specifically providing more than two drive current levels and wherein the first plurality of drive current comprises a

number n of drive current levels for the purpose of improving the quality of the display by compensating for aging effects in the display (column 2 lines 46-51).

Regarding claim 3, Inukai and Hirane, the combination discloses everything as applied above, further Inukai discloses wherein n is 8. Specifically Inukai discloses N can be any integer greater than or equal to two (column 5 lines 38-53).

Regarding claim 4, Inukai and Hirane, the combination discloses everything as applied above, in addition Inukai discloses that the first plurality of drive currents is the same as the second plurality of drive currents where the gradation of a pixel is controlled by current where the display period is selected from a group of display periods corresponding to the current and a second display period is selected from the same group of display periods (column 3 lines 41-67; figure 5A-5F).

Regarding claim 5, Inukai and Hirane, the combination discloses everything as applied above, in addition Inukai discloses that the first plurality of drive currents comprises a first number n of drive current levels for providing the lowest n non-zero brightness levels, where a first three bits (D4-D6) of a digital analog drive current value are used to provide the lowest nonzero brightness levels excluding zero brightness and where the second plurality of drive currents comprises a second number m of non-zero drive current levels for providing the higher n brightness levels, where a second three bits (D1-D3) can be used for controlling the highest brightness levels of a display to provide six combined brightness levels or n+m total brightness levels (column 3 lines 25-60; figures 5A-5C).

Regarding claim 6, Inukai and Hirane, the combination discloses everything as applied above, in addition Inukai discloses a pixel circuit with a drive transistor (108), a storage capacitor for storing a gate voltage of the drive transistor (112), and an address transistor (105) for switching a data voltage to the gate of the drive transistor during an addressing phase (figure 1B).

Regarding claims 8-12, they disclose a **method** for implementing the **apparatus** of claims 1-6. Thus, claims 8-12 are an inherent variation of claims 1-6 and are interpreted and rejected for the same reasons as stated above (see claims 1-5).

Regarding claim 13, Inukai and Hirane, the combination discloses everything as applied above, in addition Inukai discloses that the first plurality of drive currents is the same as the second plurality of drive currents, where the gradation of a pixel is controlled by current where the display period is selected from a group of display periods corresponding to the current and a second display period is selected from the same group of display periods (column 3 lines 41-67; figure 5A-5F).

Regarding claim 14, Inukai and Hirane, the combination discloses everything as applied above, in addition Inukai discloses a pixel circuit with a drive transistor (108), a storage capacitor for storing a gate voltage of the drive transistor (112), and an address transistor (105) for switching a data voltage to the gate of the drive transistor during an addressing phase (figure 1B).

Regarding claim 15, Inukai and Hirane, the combination discloses everything as applied above, further Inukai discloses wherein only the first phase is used to provide

the lowest n brightness levels (column 3 lines 25-40; column 5 lines 23-66; column 8 lines 51-55; column 9 lines 21-42; figures 5-8).

Regarding claim 16, Inukai and Hirane, the combination discloses everything as applied above, further Inukai discloses wherein only the second phase is used to provide the brightness levels higher than the lowest n brightness levels (column 3 lines 25-40; column 5 lines 23-66; column 8 lines 51-55; column 9 lines 21-42; figures 5-8).

Regarding claim 17, Inukai and Hirane, the combination discloses everything as applied above, further Inukai discloses where the first phase is used for higher resolution and the second phase is used for lower resolution(column 3 lines 25-40; column 5 lines 23-66; column 8 lines 51-55; column 9 lines 21-42; figures 5-8).

Regarding claim 18, Inukai and Hirane, the combination discloses everything as applied above, further Inukai discloses wherein a highest brightness level is provided by turning off drive currents during the first phase, and increasing a peak drive current in the second phase to a higher level than an allowable peak drive current in the first phase during gradation display (column 3 lines 25-40; column 5 lines 23-66; column 8 lines 51-55; column 9 lines 21-42; figures 5-8).

Regarding claim 19, Inukai and Hirane, the combination discloses everything as applied above, further Inukai discloses wherein all the display pixels are addressed twice within the display period (column 3 lines 25-40; column 5 lines 23-66; column 8 lines 51-55; column 9 lines 21-42; figures 5-8).

Regarding claim 20, Inukai and Hirane, the combination discloses everything as applied above, further Inukai discloses wherein all the display pixels are addressed once row by row during the first phase, and are re-addressed in a same row by row order during the second phase (column 3 lines 25-40; column 5 lines 23-66; column 8 lines 51-55; column 9 lines 21-42; figures 5-8).

Regarding claims 21-22, they disclose a **method** for implementing the **apparatus** of claims 15-16 and 18. Thus, claims 21-22 are an inherent variation of claims 15-16 and 18 and are interpreted and rejected for the same reasons as stated above (see claims 15-16 and 18).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Inukai in view of Hirane and further in view of Hack et al. (United States Patent Application Publication 2002/0030647), hereinafter referenced as Hack.

Regarding claim 7, Inukai and Hirane, the combination discloses everything as applied above, further the combination discloses the display device in claim 1, however the combination fails to disclose a portable electronic device.

In a similar field of invention Hack discloses a display in a portable electronic device (paragraph 69).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Inukai and Hirane with Hack by specifically providing a portable electronic device for the purpose of allowing a user to conveniently use a portable device with a display in a variety of locations.

Response to Arguments

4. Applicant's arguments have been considered but are not persuasive.

On pages 8-9, Applicant argues that because Inukai does not disclose wherein the first plurality of drive current comprise a number n of drive current levels, then Inukai cannot disclose the claimed "the duration of one phase is approximately n times the duration of the other phase", as Inukai fails to disclose n current levels.

The Examiner respectfully disagrees, because as cited in the rejection, Inukai discloses the current levels, including a zero drive level, and that the duration of one period is approximately n times the duration of the other phase where n is the number of drive currents that can be used in the display (figures 5A-5F; column 3 lines 25-40; column 8 lines 51-55). The n drive current levels that Inuaki does not disclose are the drive current levels where n is greater than two, i.e., there are more than two drive current levels. Inukai can disclose that the duration of one period is approximately n times (in this case two times) the duration of the other period where the number n is the same as the number of the drive current levels, i.e. two drive current levels, while not disclosing the n drive current levels where n is greater than two. Further, the claim does not recite that, "the relationship among the periods represents multiples based on the number of current levels", as described in the arguments section of Applicant's remarks. Hence the Examiner maintains that the combination is proper and would result in the invention as claimed.

On page 10, Applicant argues that because Inukai does not specifically state that n is the number of drive current levels the number n in the instant invention is different than the number n in Inukai.

The Examiner respectfully disagrees, because Inukai discloses that there are two drive current levels, which directly reads on claim 3. This number of drive current levels directly corresponds to the ratio of the lengths of the drive periods (column 5 lines 36-53). Because Inukai discloses both two drive current levels and the periods that are determined based upon this ratio, Inuaki discloses the invention as claimed. That Inukai does not state this explicitly does not mean that Inukai does not disclose this feature. Clearly Inukai discloses two drive current levels, and periods with lengths determined by this same number are disclosed in the above cited portions.

Conclusion

5. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart McCommas whose telephone number is

(571)270-3568. The examiner can normally be reached on Monday-Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on (571)272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SSM

/Alexander Eisen/

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